



Real-time Clock Module (I²C Bus)

Features

- Uses external 32.768kHz quartz crystal for PT7C4337
- Supports I²C-Bus's high speed mode (400 kHz)
- Includes time (Hour/Minute/Second) and calendar (Year/Month/Date/Day) counter functions (BCD code)
- Programmable square wave output signal
- Two Time-of-Day Alarms
- Oscillator Stop Flag
- Operating range: 1.8V to 5.5V
- Timekeeping range: 1.2V to 1.8V
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please <u>contact us</u> or your local Diodes representative.

https://www.diodes.com/quality/product-definitions/

- Packaging (Pb-free & Green)
 - 8-Pin, SOIC (W)
 - 8-Pin, MSOP (U)
 - 8-Pin, TDFN (ZE)
 - 8-Pin, TSSOP (L)

Description

The PT7C4337 serial real-time clock is a low-power clock/calendar with two programmable time-of-day alarms and a programmable square-wave output.

Address and data are transferred serially via a 2-wire, bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator.

The device is fully accessible through the serial interface while VCC is between 1.8V and 5.5V. I²C operation is not guaranteed below 1.8V. Timekeeping operation is maintained with VCC as low as 1.2V.

Table 1 shows the basic functions of PT7C4337. More details are shown in section: overview of functions.

Table 1. Basic Functions of PT7C4337

Item	Function			PT7C4337
		Source	Crystal(32.768KHz)	External crystal
1	Oscillator	Oscillator enable/	/disable	√
		Oscillator fail det	ect	√
	Time	Time	12-hour	√
		display	24-hour	√
2		Century bit		Not Supported
		Time count chain enable/disable		√
3	Interrupt	Alarm interrupt o	utput	√2
4	Programmable squ	are wave output (Hz	z)	1, 4.096k, 8.192k, 32.768k
5	Communication	2-wire I ² C bus		√

Notes:

^{1.} No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.

^{2.} See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.

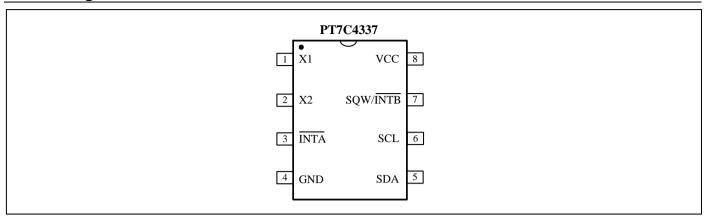
^{3.} Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.







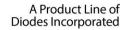
Pin Configuration



Pin Description

Pin#	Pin	Type	Description
1	X1	I	Oscillator Circuit Input. Together with X1, 32.768kHz crystal is connected between them. Or external clock input.
2	X2	О	Oscillator Circuit Output. Together with X1, 32.768kHz crystal is connected between them. When 32.768kHz external input, X2 must be float.
6	SCL	I	Serial Clock Input. SCL is used to synchronize data movement on the I ² C serial interface.
5	SDA	I/O	Serial Data Input/Output. SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open-drain output and requires an external pull-up resistor.
3	INTA	О	Interrupt Output. When enabled, INTA is asserted low when the time matches the values set in the alarm registers. This pin is an open-drain output and requires an external pull up resistor.
7	SQW/ INTB	О	Square-Wave/Interrupt Output. Programmable square-wave or interrupt output signal. It is an open-drain output and requires an external pull up resistor.
8	VCC	P	Power. Primary power for PT7C4337.
4	GND	P	Ground.
/	NC		No Connect. These pins are not connected internally, but must be grounded for proper operation.







Maximum Ratings

Storage Temperature	65°C to +150°C
Supply Voltage to Ground Potential (V _{CC} to G	ND)0.3V to +6.5V
DC Input (All Other Inputs except Vcc & GND)	-0.3V to $(V cc +0.3V)$
DC Output Voltage (SDA, /INTA, /INTB pins)	0.3V to +6.5V
DC Output Current (FOUT)	0.3V to (Vcc +0.3V)
Power Dissipation	. 320mW(depend on package)
Junction Temperature	125°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Mode

The amount of current consumed by the PT7C4337 is determined, in part, by the I^2C interface and oscillator operation. The following table shows the relationship between the operating mode and the corresponding I_{CC} parameter.

Operating Mode	V _{CC}	Power
I ² C Interface Active	$1.8V \le V_{CC} \le 5.5V$	I _{CC} Active (I _{CCA})
I ² C Interface Inactive	$1.8V \le V_{CC} \le 5.5V$	I _{CC} Standby (I _{CCS})
I ² C Interface Inactive	$1.2V \le V_{CC} \le 1.8V$	Timekeeping (I _{CCTOSC})
I ² C Interface Inactive, Oscillator Disabled	$1.2V \le V_{CC} \le 1.8V$	Data Retention (I _{CCTDDR})

Recommended Operating Conditions

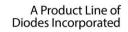
Part #	Sym.	Desc	Min	Type	Max	Unit	
	V _{CC}	V supply voltage		1.8	3.3	5.5	
	$V_{\rm CCT}$ $V_{\rm CC}$ supply voltage		1.2	-	1.8		
	V_{OSC}	Oscillator start up voltage		1.2	-	5.5	
PT7C4337	V _{IH} Input high level		SCL, SDA	0.7V _{CC}	-	V _{CC} +0.3	V
11701337		INTA , SQW/ INTB	-	-	5.5		
	V_{IL}	Input low level		-0.3	-	0.3V _C	
	T_A	Operating temperature		-40	-	85	$^{\circ}$

DC Electrical Characteristics

Unless otherwise specified, V_{CC} = 1.8~5.5V, T_A = -40 $^{\circ}C$ to +85 $^{\circ}C$

Sym.	Item	Pin	Condition	Min	Тур	Max	Unit
V _{CC}	Supply voltage	V _{CC}	Full operation	1.8	-	5.5	V
V _{CCT}	Suppry voltage	V CC	Timekeeping (Note 5)	1.2	-	1.8	
V _{OSC}	Oscillator voltage	V _{CC}		1.2	-	5.5	V
V_{IL1}	Low-level input voltage	SCL		-0.3	-	$0.3V_{CC}$	V
V_{IH1}	High-level input voltage	SCL		$0.7V_{CC}$	-	V _{CC} +0.3	V
$V_{\rm IL2}$	Low-level input voltage	X1		-	0.53	-	V
V_{IH2}	High-level input voltage	X1		-	0.53	-	V
I _{OL}	Low-level output current	SDA, /INTA, /INTB	$V_{OL} = 0.4V$	3	-	-	mA
I_{IL}	Input leakage current	SCL		-1	-	1	μΑ
I_{OZ}	Output current when OFF	SDA, /INTA, /INTB		-1	ı	1	μΑ







DC Electrical Characteristics

Sym.	Item	Pin	Condition	Min	Тур	Max	Unit			
Unless oth	Unless otherwise specified, $V_{CC} = 1.3 \sim 1.8 \text{V}$, $T_A = -40 ^{\circ}\text{C}$ to $+85 ^{\circ}\text{C}$									
I _{CCTOSC}	Timekeeping current	V _{CC}	Note 2, 4, 5	-	450	800	nA			
I_{CCTDDR}	Data retention current	V _{CC}	Note 2,4,5,6	-	-	160	пл			
Unless of	herwise specified, $V_{CC} = 1$.	$8 \sim 3.6 \text{V}, T_A = -40 ^{\circ}\text{C} \text{ to}$	+85 °C							
I_{CCA}	Active supply current	V _{CC}	Note 1, 5	-	-	100	^			
I _{CCS}	Standby current	V _{CC}	Note 2, 3, 5	-	0.6	1.0	μΑ			
Unless of	Unless otherwise specified, $V_{CC} = 3.6 \sim 5.5 \text{V}$, $T_A = -40 ^{\circ}\text{C}$ to $+85 ^{\circ}\text{C}$									
I_{CCA}	Active supply current	V _{CC}	Note 1, 5	-	-	150	^			
I _{CCS}	Standby current	V _{CC}	Note 2, 3, 5	-	1.0	1.8	μΑ			

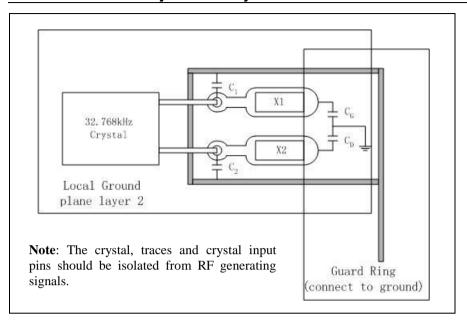
Note:

- SCL clocking at max frequency = 400 kHz, $V_{IL} = 0.0 V$, $V_{IH} = VCC$. Specified with 2-wire bus inactive, $V_{IL} = 0.0 V$, $V_{IH} = VCC$. 1.
- 2.
- SQW enabled.
- $\widetilde{Spec}\mbox{ified}$ with the SQW function disabled by setting $\mbox{INTCN}=1.$ 4. 5.
- Using recommended crystal on X1 and X2. Crystal oscillator is disabled.
- 6.





Recommended Layout for Crystal



Built-in Capacitors Specifications and Recommended External Capacitors

Parameter	Parameter			Unit
Duild in conscitous	X1 to GND	C_{G}	12	pF
Build-in capacitors	X2 to GND	C_D	12	pF
Recommended External capacitors for	X1 to GND	C ₁	13	pF
crystal C _L =12.5pF	X2 to GND	C_2	13	pF
Recommended External capacitors for crystal C_L =6pF	X1 to GND	C ₁	0	pF
	X2 to GND	C_2	0	pF

Note: The frequency of crystal can be optimized by external capacitor C_1 and C_2 , for frequency=32.768KHz, C_1 and C_2 should meet the equation as below:

 $Cpar + [(C_1+C_G)*(C_2+C_D)]/[(C_1+C_G)+(C_2+C_D)] = C_L$

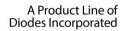
Cpar is all parasitical capacitor between X1 and X2.

C_L is crystal's load capacitance.

Crystal Specifications

Parameter	Symbol	Min	Тур	Max	Unit
Nominal Frequency	f_{O}	-	32.768	-	kHz
Series Resistance	ESR	-	-	70	kΩ
Load Capacitance	C_{L}	-	6/12.5	-	pF

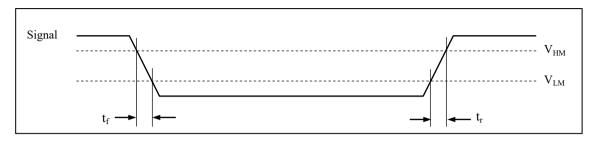






AC Electrical Characteristics

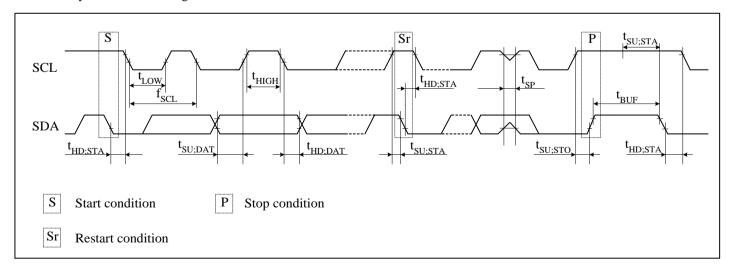
Ī	Sym	Description	Value	Unit
Ī	V_{HM}	Rising and falling threshold voltage high	$0.8~\mathrm{V_{CC}}$	V
ſ	V_{HL}	Rising and falling threshold voltage low	$0.2~\mathrm{V_{CC}}$	V



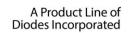
Over the operating range

Symbol	Item	Min.	Тур.	Max.	Unit
f_{SCL}	SCL clock frequency	-	-	400	kHz
t _{SU;STA}	START condition set-up time	0.6	-	-	μs
t _{HD;STA}	START condition hold time	0.6	-	-	μs
t _{SU;DAT}	Data set-up time (RTC read/write)	200	-	-	ns
t _{HD;DAT1}	Data hold time (RTC write)	35	-	-	ns
t _{HD;DAT2}	Data hold time (RTC read)	0	-	-	μs
t _{SU;STO}	STOP condition setup time	0.6	-	-	μs
t _{BUF}	Bus idle time between a START and STOP condition	1.3	-	-	μs
t_{LOW}	When SCL = "L"	1.3	-	-	μs
t _{HIGH}	When SCL = "H"	0.6	-	-	μs
t _r	Rise time for SCL and SDA	-	-	0.3	μs
$t_{\rm f}$	Fall time for SCL and SDA	-	-	0.3	μs
t _{SP} *	Allowable spike time on bus	-	-	50	ns
C _B	Capacitance load for each bus line	-	-	400	pF
C _{I/O} *	I/O Capacitance (SDA, SCL)	-	-	10	pF
T _{OSF}	Oscillator Stop Flag (OSF) Delay	-	-	100	ms

^{*} Note: only reference for design

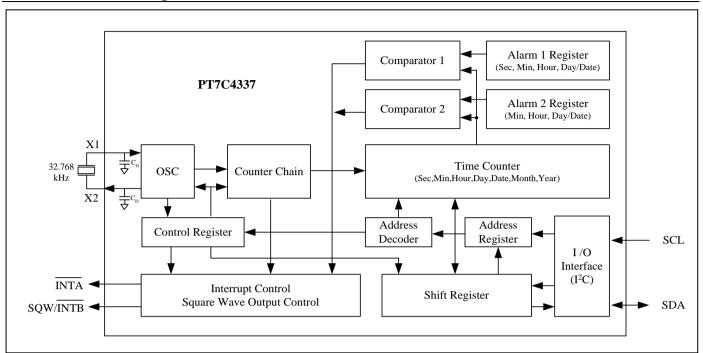








Function Block Diagram



Oscillator Circuit

PT7C4337

The PT7C4337 uses an external 32.768 kHz crystal. Table2 specifies several crystal parameters for the external crystal. The *Block Diagram* shows a functional schematic of the oscillator circuit. The startup time is usually less than 1 second when using a crystal with the specified characteristics.

Table 2 Crystal Specifications

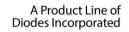
Parameter	Symbol	Min	Тур	Max	Unit
Nominal Frequency	f_{O}	-	32.768	-	kHz
Series Resistance	ESR	-	-	70	kΩ
Load Capacitance	C_{L}	-	6/12.5	-	pF

Note: The crystal, traces, and crystal input pins should be isolated from RF generating signals.

Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Crystal frequency drift caused by temperature shifts creates additional error. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 1 shows a typical PC board layout for isolating the crystal and oscillator from noise.







Function Description

Overview of Functions

Clock Function

CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2100.

Alarm Function

This device has two alarm system (Alarm 1 and Alarm 2) that outputs interrupt signals from INTA or INTB to CPU when the date, day of the week, hour, minute or second correspond to the setting. Each of them may output interrupt signal separately at a specified time. The alarm is be selectable between on and off for matching alarm or repeating alarm.

Programmable Square Wave Output

A square wave output enable bit controls square wave output at pin 7. Frequencies are selectable: 1, 4.096k, 8.192k, 32.768k Hz.

Interface with CPU

Data is read and written via the I²C bus interface using two signal lines: SCL (clock) and SDA (data).

Since the output of the I/O pin SDA is open drain, a pull-up resistor should be used on the circuit board if the CPU output I/O is also open drain.

The SCL's maximum clock frequency is 400 kHz, which supports the I²C bus's high-speed mode.

Oscillator Fail Detect

When oscillator fail, PT7C4337 OSF bit will be set.

Oscillator enable/disable

Oscillator and time count chain can be enabled or disabled at the same time by /ETIME bit.

Registers

Allocation of Registers

Addr.	E4'				Register l	Definition			
(hex)*1	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Seconds (00-59)	0	S40	S20	S10	S 8	S4	S2	S1
01	Minutes (00-59)	0	M40	M20	M10	M8	M4	M2	M1
02	Hours (00-23 / 01-12)	0	12, /24	H20 or P, /A	H10	Н8	H4	H2	H1
03	Days of the week (01-07)	0	0	0	0	0	W4	W2	W1
04	Dates (01-31)	0	0	D20	D10	D8	D4	D2	D1
05	Months (01-12)	0	0	0	MO10	MO8	MO4	MO2	MO1
06	Years (00-99)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
07	Alarm 1: Seconds	A1M1*2	S40	S20	S10	S8	S4	S2	S1
08	Alarm 1: Minutes	A1M2*2	M40	M20	M10	M8	M4	M2	M1
09	Alarm 1: Hours	A1M3*2	12, /24	H20 or P, /A	H10	Н8	H4	H2	H1
0A	Alarm 1: Day, Date	A1M4*2	Day, /Date	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
0B	Alarm 2: Minutes	A2M2*3	M40	M20	M10	M8	M4	M2	M1
0C	Alarm 2: Hours	A2M3*3	12, /24	H20 or P, /A	H10	Н8	H4	H2	H1
0D	Alarm 2: Day, Date	A2M4*3	Day, /Date	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
0E	Control	/ETIME*4	0	0	RS2*5	RS1*5	INTCN*6	A2IE*7	A1IE*7
0F	Status	OSF ^{*9}	0	0	0	0	0	A2F*8	A1F*8







Caution Points:

- *1. PT7C4337 uses 8 bits for address. For excess 0FH address, PT7C4337 will not respond (no acknowledge signal was given).
- *2. Alarm 1 mask bits. Select alarm repeated rate when an alarm occurs.
- *3. Alarm 2 mask bits. Select alarm repeated rate when an alarm occurs.
- *4. Oscillator and time count chain enable/disable bit.
- *5. Square wave output frequency select.
- *6. Interrupt output pin select bit.
- *7. Alarm 1 and alarm 2 enable bits.
- *8. Alarm 1 and alarm 2 flag bits.
- *9. Oscillator stop flag.
- *10. All bits marked with "0" are read-only bits. Their value when read is always "0".

Control and Status Register

002202	or arra Status rec	5-200-							
Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
0E	Control	/ETIME	0	0	RS2	RS1	INTCN	A2IE	A1IE
UE	(default)	0	0	0	1	1	0	0	0
0F	Status	OSF	0	0	0	0	0	A2F	A1F
UF	(default)	1	0	0	0	0	0	Undefined	Undefined

Oscillator Related Bits

/ETIME

Enable oscillator and time count chain bit.

/ETIME	Data	Description	
Read / Write	0	Enable oscillator and time count chain.	Default
Read / Wille	1	Disable oscillator and time count chain.	

OSF

Oscillator Stop Flag.

A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and may be used to judge the validity of the clock and calendar data. This bit is set to logic 1 anytime that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

- 1) The first time power is applied.
- 2) The voltage present on VCC is insufficient to support oscillation.
- 3) The /ETIME bit is turned off.
- 4) External influences on the crystal (e.g., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0.

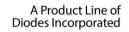
Square Wave Frequency Selection Bits

RS2, RS1

Square wave Rate Select. These bits control the frequency of the square-wave output when the square wave has been enabled.

RS2, RS1	Data	SQW output freq. (Hz)
	00	1
Read / Write	01	4.096k
Read / Wille	10	8.192k
	11	32.768k Default







Interrupt related bits

INTCN

Interrupt Output pin select bit. This bit controls the relationship between the two alarms and the interrupt output pins.

INTCN	Data	Description
Read /	1	A match between the timekeeping registers and the alarm 1 registers activates the INTA pin (if the alarm 1 is enabled) and a match between the timekeeping registers and the alarm 2 registers activates the SQW/INTB pin (if the alarm 2 is enabled).
Write	0	A match between the timekeeping registers and either alarm 1 or alarm 2 registers activates the INTA pin (if the alarms are enabled). In this configuration, a square wave is output on the SQW/INTB pin.

A1IE

Alarm 1 Interrupt Enable.

A1IE	Data	Description					
Read /	0	The A1F bit does not initiate the INTA signal.	Default				
Write	1	Permits the alarm 1 flag (A1F) bit in the status register to assert INTA.					

• A1F

Alarm 1 Flag.

marin i i iag.			
A1F	Data	Description	
Read / Write	0	The time do not match the alarm 1 registers. Defa	ıult
Read	1	Indicates that the time matched the alarm 1 registers. If the A1IE bit is also logic 1, the INTA pin goes low. A1F is cleared when written to logic 0. Attempting to write to logic 1 leaves the value unchanged.	

• **A2IE**

Alarm 2 Interrupt Enable.

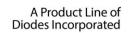
A2IE	Data	Description	
	0	The A2F bit does not initiate an interrupt signal. Defa	ault
Read / Write	1	Permits the alarm 2 flag (A2F) bit in the status register to assert INTA (when INTCN = 0) or to assert	sert
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	1	$\overline{SQW/INTB}$ (when INTCN = 1).	

• A2F

Alarm 2 Flag.

A1F	Data	Description
Read / Write	0	The time do not match the alarm 2 registers. Defaul
Read	1	Indicates that the time matched the alarm 1 registers. This flag can be used to generate an interrupt on either INTA or SQW/INTB depending on the status of the INTCN bit. If the INTCN = 0 and A2F = 1 (and A2IE = 1), the INTA pin goes low. If the INTCN = 1 and A2F = 1 (and A2IE = 1), the SQW/INTB pin goes low. A2F is cleared when written to logic 0. Attempting to write to logic 1 leaves the value unchanged.







Time Counter

Time digit display (in BCD code):

- Second digits: Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.
- Minute digits: Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.
- Hour digits: See description on the /12, 24 bit. Carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
00	Seconds	0	S40	S20	S10	S8	S4	S2	S1
00	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
01	Minutes	0	M40	M20	M10	M8	M4	M2	M1
01	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
02	Hours	0	12, /24	H20 or P,/A	H10	Н8	H4	H2	H1
02	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Note: Any registered imaginary time should be replaced with correct time, otherwise it will cause the clock counter malfunction.

• 12, /24 bit

This bit is used to select between 12-hour clock system and 24-hour clock system.

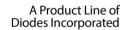
12, /24	Data	Description
Read / Write	0	24-hour system
Read / Write	1	12-hour system

This bit is used to select between 12-hour clock operation and 24-hour clock operation.

12, /24	Description	Hours register					
		24-hour clock	12-hour clock	24-hour clock	12-hour clock		
		00	52 (AM 12)	12	72 (PM 12)		
0	24 hove time display	01	41 (AM 01)	13	61 (PM 01)		
0	24-hour time display	02	42 (AM 02)	14	62 (PM 02)		
		03	43 (AM 03)	15	63 (PM 03)		
		04	44 (AM 04)	16	64 (PM 04)		
		05	45 (AM 05)	17	65 (PM 05)		
		06	46 (AM 06)	18	66 (PM 06)		
		07	47 (AM 07)	19	67 (PM 07)		
1	12 hazartina diantan	08	48 (AM 08)	20	68 (PM 08)		
1	12-hour time display	09	49 (AM 09)	21	69 (PM 09)		
		10	50 (AM 10)	22	70 (PM 10)		
		11	51 (AM 11)	23	71 (PM 11)		

^{*} Be sure to select between 12-hour and 24-hour clock operation before writing the time data.







Days of the Week Counter

The day counter is a divide-by-7 counter that counts from 01 to 07 and up 07 before starting again from 01. Values that correspond to the day of week are user defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D 0
03	Days of the week	0	0	0	0	0	W4	W2	W 1
03	(default)	0	0	0	0	0	Undefined	Undefined	Undefined

Calendar Counter

The data format is BCD format.

• Day digits: Range from 1 to 31 (for January, March, May, July, August, October and December).

Range from 1 to 30 (for April, June, September and November).

Range from 1 to 29 (for February in leap years).

Range from 1 to 28 (for February in ordinary years).

Carried to month digits when cycled to 1.

- Month digits: Range from 1 to 12 and carried to year digits when cycled to 1.
- Year digits: Range from 00 to 99 and 00, 04, 08, ..., 92 and 96 are counted as leap years.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D 0
04	Dates	0	0	D20	D10	D8	D4	D2	D1
04	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
05	Months	0	0	0	M10	M8	M4	M2	M1
03	(default)	0	0	0	Undefined	Undefined	Undefined	Undefined	Undefined
06	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
00	(default)	Undefined							

Alarm Register

• Alarm 1, Alarm 2 Register

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
07	Alarm 1: Seconds	$A1M1^{*1}$	S40	S20	S10	S 8	S4	S2	S1
07	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
08	Alarm 1: Minutes	$A1M2^{*1}$	M40	M20	M10	M8	M4	M2	M1
08	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
09	Alarm 1: Hours	A1M3*1	12, /24	H20 or P,/A	H10	Н8	H4	H2	H1
09	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
	Alarm 1: Day, Date	A1M4*1	Day, /Date ^{*1}	0,	0,	0,	W4,	W2,	W1,
0A	marin 1. Buy, Bute	7 1 1 1 1	/Date ^{**1}	D20	D10	D8	D4	D2	D1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0B	Alarm 2: Minutes	$A2M2^{*2}$	M40	M20	M10	M8	M4	M2	M1
UB	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0C	Alarm 2: Hours	A2M3*2	12, /24	H20 or P,/A	H10	Н8	H4	H2	H1
UC.	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
	A1 2. D D.t.	A2M4*2	Day,	0,	0,	0,	W4,	W2,	W1,
0D	Alarm 2: Day, Date	AZIVI4	Day, /Date ^{*2}	D20	D10	D8	D4	D2	D1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

^{*1} Note: Alarm mask bit, using to select Alarm 1 alarm rate.

^{*2} Note: Alarm mask bit, using to select Alarm 2 alarm rate.







Alarm Function Related Register

Addr.	Function				Register	definition			
(hex)	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Seconds	0	S40	S20	S10	S8	S4	S2	S1
01	Minutes	0	M40	M20	M10	M8	M4	M2	M1
02	Hours	0	12, /24	H20 or A, /P	H10	Н8	H4	H2	H1
03	Days of the week	0	0	0	0	0	W4	W2	W1
04	Dates	0	0	D20	D10	D8	D4	D2	D1
07	Alarm 1: Seconds	A1M1	S40	S20	S10	S8	S4	S2	S1
08	Alarm 1: Minutes	A1M2	M40	M20	M10	M8	M4	M2	M1
09	Alarm 1: Hours	A1M3	12, /24	H20 or A, /P	H10	Н8	H4	H2	H1
0A	Alarm 1: Day, Date	A1M4	Day, /Date	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
0B	Alarm 2: Minutes	A2M2	M40	M20	M10	M8	M4	M2	M1
0C	Alarm 2: Hours	A2M3	12, /24	H20 or A, /P	H10	Н8	H4	H2	H1
0D	Alarm 2: Day, Date	A2M4	Day,	0,	0,	0,	W4,	W2,	W1,
UD	Alaini 2. Day, Date	A21V14	/Date	D20	D10	D8	D4	D2	D1
0E	Control	/ETIME	0	0	RS2	RS1	INTCN	A2IE	A1IE
0F	Status	OSF	0	0	0	0	0	A2F	A1F

Note: Alarm function does not support different hour system adopted in time and alarm register.

The PT7C4337 contains two time-of-day/date alarms. The alarms can be programmed (by the INTCN bit of the control register) to operate in two different modes - each alarm can drive its own separate interrupt output or both alarms can drive a common interrupt output. Bit 7 of each of the time-of-day/date alarm registers are mask bits.

When all of the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers $00h \sim 04h$ match the values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 2 and Table 3 shows the possible settings.

The Day, /Date bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits $0 \sim 5$ of that register reflects the day of the week or the date of the month. If the bit is written to logic 0, the alarm is the result of a match with date of the month. If the bit is written to logic 1, the alarm is the result of a match with day of the week.

When the PT7C4337 register values match alarm register settings, the corresponding alarm flag (A1F or A2F) bit is set to logic 1. If the corresponding alarm interrupt enable (A1IE or A2IE) is also set to logic 1, the alarm condition activates one of the interrupt output (INTA or SQW/INTB) signals. The match is tested on the once-per-second update of the time and date registers.







Table 1. Alarm 1 Mask Bits

Day,	Ala	rm 1 regis	ster mask	bits	Alarm Rate
/Date	A1M4	A1M3	A1M2	A1M1	Alariii Rate
×	1	1	1	1	Alarm once per second
×	1	1	1	0	Alarm when seconds match
×	1	1	0	0	Alarm when minutes and seconds match
×	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match
		Others			Ignored.

Table 2. Alarm 2 Mask Bits

Day,	Alarn	arm 2 register mask bits		Alarm Rate
/Date	A2M4	A2M3	A2M2	Alariii Kate
×	1	1	1	Alarm once per minute (00 seconds of every minute)
×	1	1	0	Alarm when minutes match
×	1	0	0	Alarm when hours, minutes
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match
	(Others		Ignored.







I²C Bus Interface

Overview of I²C-BUS

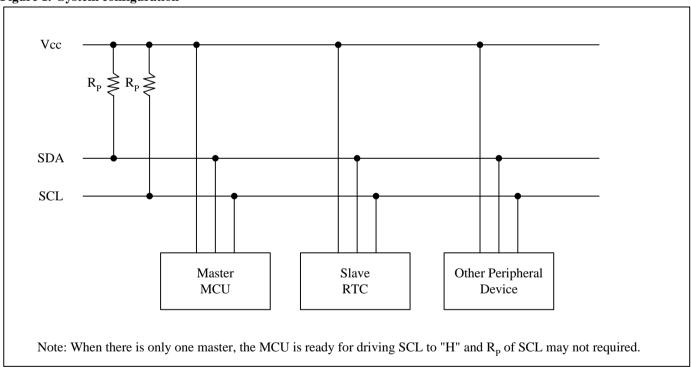
The I²C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data signals, acknowledge signals, and so on. Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level. During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is captured while the SCL line is at high level. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse. The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data.

System Configuration

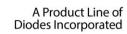
All ports connected to the I²C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.

SCL and SDA are both connected to the VDD line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).

Figure 1. System configuration



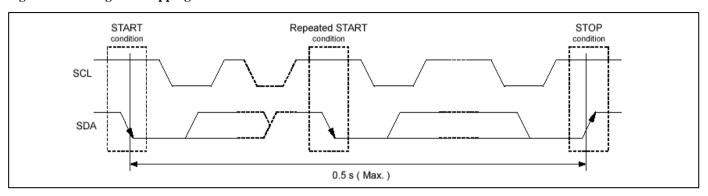






Starting and Stopping I²C Bus Communications

Figure 2. Starting and Stopping on I²C Bus



1) START Condition, Repeated START Condition, and STOP Condition

- a) START condition
 - SDA level changes from high to low while SCL is at high level
- b) STOP condition
 - SDA level changes from low to high while SCL is at high level
- c) Repeated START condition (RESTART condition)

In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

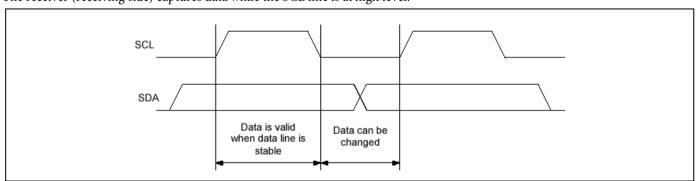
2) Data Transfers and Acknowledge Responses during I²C-BUS Communication

a) Data Transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.

The address auto increment function operates during both write and read operations.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level. The receiver (receiving side) captures data while the SCL line is at high level.

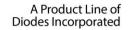


^{*}Note with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

b) Data Acknowledge Response (ACK signal)

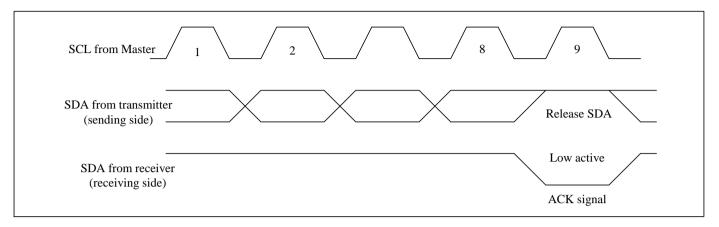
When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)







Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.



After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.

When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

Slave Address

The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.

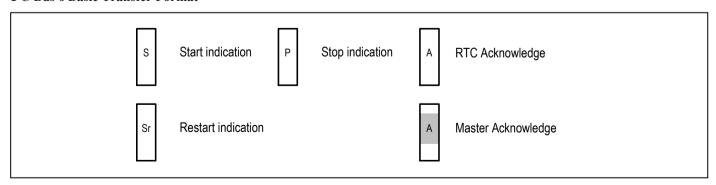
All communications begin with transmitting the [START condition] + [slave address (+ R/W specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.

Slave addresses have a fixed length of 7 bits. See table for the details.

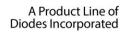
An R/\overline{W} bit is added to each 7-bit slave address during 8-bit transfers.

Onevation	Transfer data			Sla	ave addre	ess			R / W bit
Operation	Transfer data	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	D1 h	1	1	0	1	0	0	0	1 (= Read)
Write	D0 h	1	1	U	1	U	U	U	0 (= Write)

I²C Bus's Basic Transfer Format







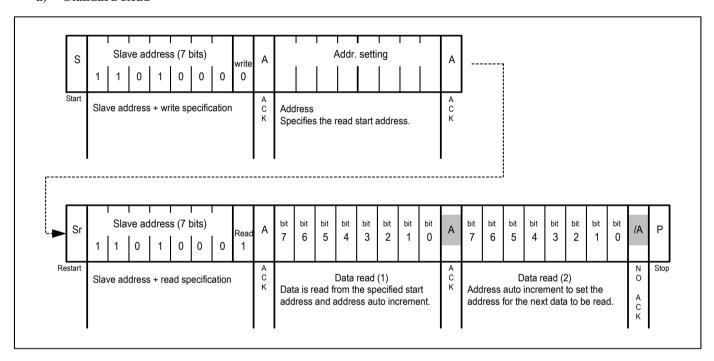


1) Write via I²C Bus

s		Slav	e ac	dres	s (7	bits)		write	Α	·	Α	ddr.	settin	g	•	•	Α	bit	bit 6	bit 5		bit 3	bit 2	bit	bit	Α	Р
	1	1	0	1	0	0	0	0										<i>'</i>	0	5	4	3			U		
Start	Slav	ve ad	dress	s + wr	ite sp	ecific	ation		A C K	Add Spe		write	start	addr	ess.		A C K	Wri	te da	ta						ACK	Stop

2) Read via I²C Bus

a) Standard Read



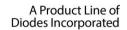
b) Simplified Read

s	Slave add	1 1	its) 0	Read 1	Α	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Α	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	/A	Р
Start	Slave address	+ read spe	ecificatio	n	A C K	by tl	he int	ead fr ternal	Data rom the address incren	ie add	dress			A C K		addre	D regist		to inc	reme			N O A C K	Stop

Note:

- 1. The above steps are an example of transfers of one or two bytes only. There is no limit to the number of bytes transferred during actual communications.
- 2. 49H, 4AH are used as test mode address. Customer should not use the addresses.







Part Marking

W Package

PT7C 4337WE XYWXX

1st X: Die Rev Y: Date Code (Year) W: Date Code (Workweek) 2nd X: Assembly Site Code 3rd X: Fab Site Code

U Package PT7C4337UE-36

P17C4337UE-36

7C43 37UE TYWXX

T: Die Rev

Y: Date Code (Year) W: Date Code (Workweek)

1st X: Assembly Site Code (Variable) 2nd X: Wafer Fab Site Code (Variable)

ZE Package



jF: PT7C4337ZEE 1st X: Die Rev Y: Date Code (Year) W: Date Code (Workweek) 2nd X: Assembly Site Code 3rd X: Fab Site Code

L Package

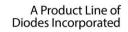
7C43 37LE • XABJW

7C4337LE: Marking ID

XAB: Die Rev/Year and Workweek of Mold Operation

J: Assembly Site Code W: Wafer Fab Site Code

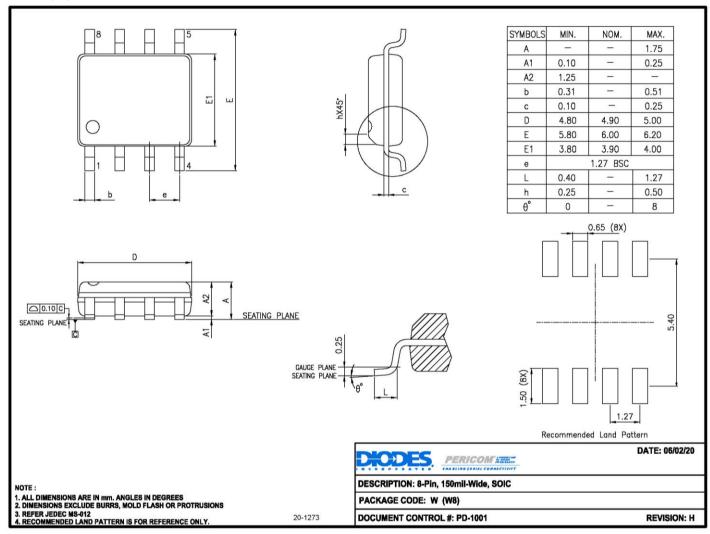




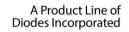


Packaging Mechanical

8-SOIC (W)









Max

1.10

0.15

0.95

0.38

0.23

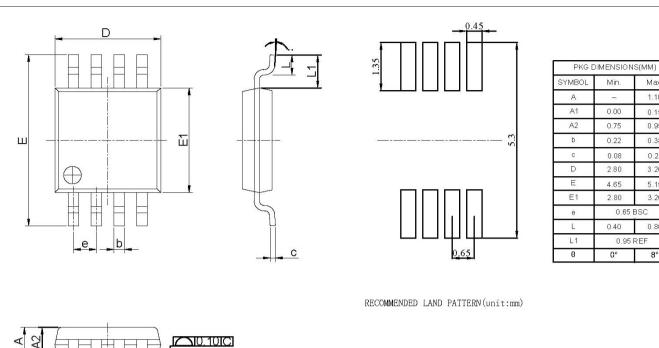
3.20

5.15

3.20

8°

8-MSOP (U)



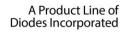


- 1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
- 2. REFER JEDEC MO-187FIAB
 3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR.
 4. LAND PATTERN REFERENCE DIODES MSOP-8 PACKAGE INFORMATION.

DECDES PERICON STRUCTURE PROPERTY PROPE	DATE: 11/04/19
DESCRIPTION: 8-Pin, Mini Small Outline Package, MSC)P
PACKAGE CODE: U (U8)	
DOCUMENT CONTROL #: PD-1261	REVISION: H

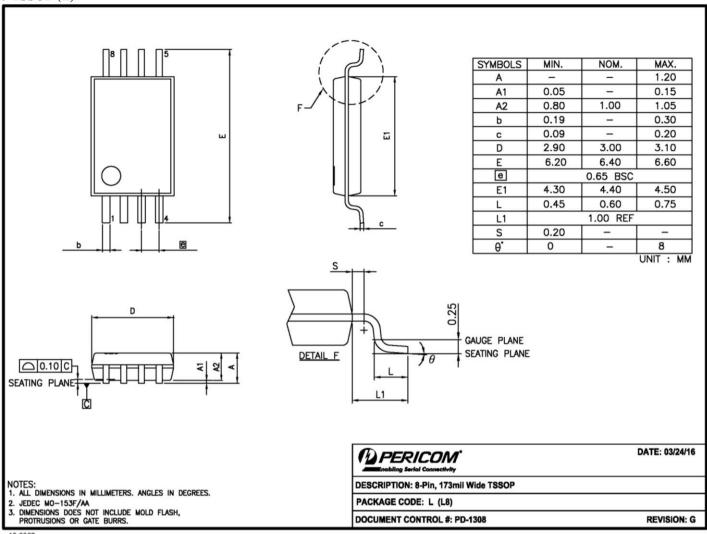
19-1147



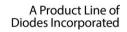






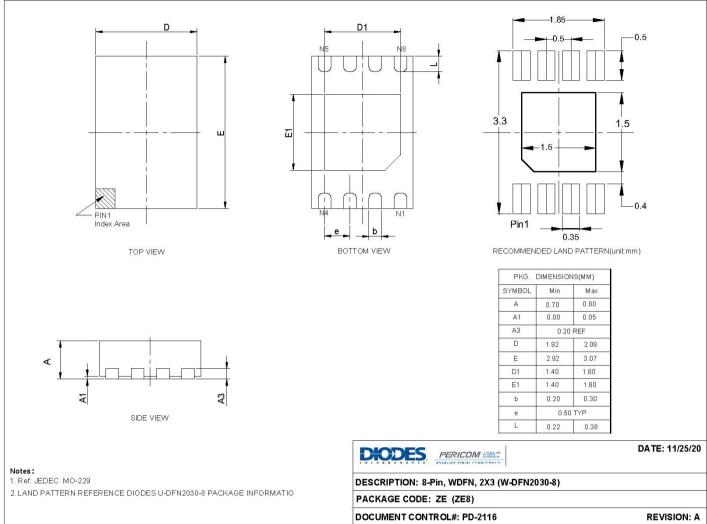








8- TDFN (ZE)



20-1348

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Part Number	Package Code	Package Description
PT7C4337WEX	W	8-Pin, 150mil-Wide (SOIC)
PT7C4337UEX	U	8-Pin, Mini Small Outline Package (MSOP)
PT7C4337LEX	L	8-Pin, 173mil Wide (TSSOP)
PT7C4337ZEEX	ZE	8-Pin, 2x3 (WDFN)

Notes:

- ${\tt No~purposely~added~lead.~Fully~EU~Directive~2002/95/EC~(RoHS),~2011/65/EU~(RoHS~2)~\&~2015/863/EU~(RoHS~3)~compliant.}\\$
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Shenzhen Zhixinke Technology Co., Ltd.



阻容器件

插件电解电容	贴片铝电解电容	贴片电容 MLCC	钽电容	薄膜电容
贴片电阻	热敏电阻	压敏电阻	碳膜电阻	金属膜电阻

高压MOS(N-400V N-500V N-600V N-650V N-700V N-800V N-900V / 电流: 0.5A~26A区间 电压电流选型)

2N65 650V	2A	T0-252	7N60	600V	7A	T0-252	8N65	650V	8A	T0-251	10N50	500V	10A	T0-220F	15N50	500V	15A	TO-220F	
4N65 650V	4A	TO-220F	7N65	650V	7A	TO-220F	8N65	650V	8A	T0-252	12N65	650V	12A	TO-220F	15N65	650V	15A	TO-220F	
5N60 600V	5A	TO-220F	7N65	650V	7A	T0-252	8N65	650V	8A	T0-252	12N70	700V	12A	TO-220F	15N70	700V	10A	TO-220F	
5N65 650V	5A	T0-252	7N70	700V	7A	TO-220F	9N70	700V	9A	T0-252	13N50	500V	13A	T0-220F	20N50	500V	20A	T0-220F	

低压MOS (电流: -160A~300A区间选型)

N+P 20V	P -100V	Dual N 30V	N 30V	N 75V
N+P 30V	P -12V	Dual N 100V	N 40V	N 85V
N+P 40V	P -16V	Dual N 20V	N 55V	N 100V
Dual P -30V	P -20V	Dual N 40V	N 60V	N 150V
Dual P -60V	P -40V	N 20V	N 68V	N 200V

二极管专业制造商(定制产品,需要一周~二周时间)参数查看选型表

超低正向肖特基整流二极管	肖特基整流二极管	普通整流二极管	快恢复整流二极管	高效整流二极管
超快恢复整流二极管	双向触发二极管	瞬变电压抑制二极管	稳压二极管	桥式整流器
小信号肖特基二极管	小信号开关二极管	光伏二极管	汽车整流器	高压触发管

桥式整流器专业制造(定制产品,需要一周~二周时间)

芯片尺寸/类别
50MIL DBS
60MIL DBS
60MIL DBS
70MIL DBS
50MIL DB
60MIL DB
60MIL DB
70MIL DB
50MIL KBP
60MIL KBP
70MIL KBP
50MIL GBP短脚
60MIL GBP短脚
70MIL GBP短脚
84MIL GBP短脚
88MIL GBP短脚
50MIL GBP长脚
60MIL GBP长脚
70MIL GBP长脚
84MIL GBP长脚
88MIL GBP长脚
60MIL D3K
70MIL D3K
84MIL D3K
70MIL KBL
84MIL KBL
88MIL KBL
70MIL GBU
84MIL GBU



DB-S



KBP



GBP



D3K



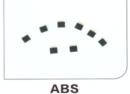
型号 芯片尺寸/类别 GBU606-GBU610 88MIL GBU806-GBU810 95MIL GBU GBU1006-GBU1010 100MIL GBU GBU1506-GBU1510 GBU 110MILGBU2506-GBU2510 130MIL GBU GBJ406-410 84MIL 4GB.J GBJ606-610 88MIL 4GBJ GBJ806-810 95MIL 4GB.J GBJ1006-1010 100MIL 4GB.J GBJ1506-1510 110MIL 4GB.J GBJ2506-2510 130MIL 4GBJ GBJ1506-1510 110MIL 6GBJ GBJ1506-1510 120MIL 6GBJ GBJ2506-2510 130MIL 6GBJ GBJ3506-3510 140MTL 6GBJ GBJ3506-3510 160MIL 6GBJ KBJ406-410 84MIL KBJ (4GBJ) KBJ606-610 **88MIL** KBJ (4GBJ) KBJ806-810 95MIL KBJ (4GBJ) KBJ1006-1010 100MIL KBJ (4GBJ) KBJ (4GBJ) KBJ1506-1510 110MIL KBJ2506-2510 KBJ (4GBJ) 130MIL MB6S-10S 46MIL **MBS** MB6S-10S 50MIL **MBS** MB6F-10F 46MIL **MBF** MB6F-10F 50MIL **MBF** ABS6-ABS10 46MIL ABS ABS6-ABS10 50MIL **ABS** ABS6-ABS10 60MIL ABS











深圳市致新科科技有限公司

Shenzhen Zhixinke Technology Co., Ltd.



光耦 红外对射

EL0631	EL814	LTV-217	KAQY212	MOC3022
EL1018	EL817	LTV-247	KMOC3021	MOC3023
EL1019	ELM440A	LTV-3063	KMOC3022	MOC3042
EL2501	ELM453	LTV-3223	KMOC3023	MOC3052
EL3041	ELM611	LTV-356	KMOC3041	MOC3063
EL3063	ELQ3H4	LTV-357	KMOC3042	MOC3043
EL354	ELQ3H7	LTV-814	KMOC3043	HS0038BD
EL357	ELR3223	LTV-816	KMOC3063	IR204C-A-L
EL3H4	ELS3120	LTV-817	KMOC3083	IR333C-A
EL3H7	ELS3150	CT3043	FOD814	ITR1100
EL406A	ELS680	CT3063	6N137	ITR8102
EL6N137	CT3023	CTT3223	MOC3021	ITR8402

长晶 JSCJ (原名长电)

1N4148WS	SOD323	BC547	T092	BZT52C3V6	SOD123	CJ431	SOT-23	MMBT3904	SOT23
2N5551	TO-92	BC548	T092	BZT52C3V9	SOD123	СЈ7812	T0220-3L	MMBT540	SOT23
2SA1013	S0T89-3L	BCX56-16	S0T89-3L	BZT52C5V1	SOD123	СЈ7815	T0252-2L	MMBTA44	SOT-23
2SB1386	SOT89	BD237	T0126	BZT52C6V2	SOD123	CJ78L05	S0T89	MMBTA94	SOT23
2SC1623	SOT23	BSS123	S0T23	BZT52C6V8S	SOD323	CJ78L08	S0T89	MMSZ4689	SOD123
2SC1815	T092	BU406	T0220-3L	BZT52C8V2	SOD123	CJ78L12	S0T89	RS3M	SMBG
2SC2712	SOT-23	BZT52C10	SOD123	BZX84C15	S0T23	CJ78M05	T0252	S8050	SOT23
2SD1724	T0-126	BZT52C12	SOD123	C1815	T092F	CJ78M06	T0252	S8550	SOT23
2SD965A	SOT89	BZT52C15	SOD123	CJ2301	S0T23	CJ78M12	T0252	S9012	SOT23
B0530WS	SOD323	BZT52C18	SOD123	CJ2302	S0T23-3	CJ79L05	T092	S9013	SOT23
B5819W	SOD123	BZT52C22S	SOD323	СЈ2304	SOT-23	D882	T0126	S9014	SOT23
BAT54	S0T23-3	BZT52C24V	SOD123	СЈ2306	S0T23	ES2J	SMAG	S9015	SOT23
BAV99	SOT23	BZT52C30	SOD123	СЈ2310	SOT23	LM317	S0T223	SD103AW	SOD123
BC546B	T092	BZT52C3V3	SOD123	СЈ3415	S0T23-3	MCR100-8	T092	TIP122	T0126

圣邦微 (SGMICRO)

SGM2019	SGM3110-5. OYN6/TR	SGM4056-6.8YPS8G/TR	SGM6232YPS8G/TR	SGM809
SGM2021	SGM3132YDE8G/TR	SGM4056-6.8YTDE8G/TR	SGM6603	SGM810
SGM2032	SGM3157YC6/TR	SGM4062YDE8G/TR	SGM6609YTDF12G/TR	SGM8272YS8G/TR
SGM2033	SGM3206YN5G/TR	SGM4064YDE8G/TR	SGM706	SGM8522XS/TR
SGM2036	SGM321YN5/TR	SGM44599YTQ16/TR	SGM721XN5/TR	SGM8582XS8G/TR
SGM2200	SGM324YS14/TR	SGM4582YTS16G/TR	SGM7222YMS10/TR	SGM8632XMS/TR
SGM2203	SGM330A-YQS/TR	SGM4807YTDE8G/TR	SGM7222YWQ10/TR	SGM8632XS/TR
SGM2268YWQ10/TR	SGM331A-YQS16G/TR	SGM4871YPS8/TR	SGM7227YMS10G/TR	SGM8634XS14/TR
SGM2549YN6G/TR	SGM358YMS/TR	SGM4890YMS/TR	SGM7227YUWQ10G/TR	SGM89000YTS14G/TR
SGM2551AYN5G/TR	SGM358YS/TR	SGM4891YDE8G/TR	SGM7228YWQ10G/TR	SGM8903YTS14G/TR
SGM2554AYN5G/TR	SGM3700YTQ16G/TR	SGM4917AYTQ16G/TR	SGM722XMS/TR	SGM8904YMS10G/TR
SGM2571ADYG/TR	SGM3732YTN6G/TR	SGM4918AYD10G/TR	SGM722XS/TR	SGM9111YC5/TR
SGM2576YN5G/TR	SGM3733BYTDI6G/TR	SGM4996YMS8G/TR	SGM8051XN5/TR	SGM9114YN6G/TR
SGM2578YG/TR	SGM3752YTN6G/TR	SGM6012	SGM8054XS/TR	SGM9116XS/TR
DIODEC(美女) DAN 五年	引速 (= -=			

DIODES(美台) PAM 百利通(pericom)

AL1666S-13	AL8863SP-13	APT17NTR-G1	PAM2861ABR	PAM8403DR-H
AL1692-30BS7-13	AP1084D25G-13	AS78L05RTR-E1	PAM2861CBR	PAM8404KGR
AL1692S-13	AP1084D33G-13	AZ1117	PAM2863ECR	PAM8406DR
AL1697-40DS7-13	AP1501-50K5G-13	AZ34063UMTR-G1	PAM8003DR	PAM8610TR
AL17050WT-7	AP1501-K5G-13	AZ431AN-ATRE1	PAM8004DR	PAM8620TR
AL3353S-13	AP1603WG-7	PAM2301CAABADJ	PAM8006ATR	PAM8902HKER
AL5812MP-13	AP2127K-ADJTRG1	PAM2305AABADJ	PAM8007NHR	PAM8904JER
AL8805W5-7	AP2204K-3.3TRG1	PAM2305CGFADJ	PAM8106TVR	PAM8908JER
AL8807W5-7	AP2204K-5. 0TRG1	PAM2312AABADJ	PAM8124RHR	PAM8908JER
AL8808WT-7	AP2204K-ADJTRG1	PAM2401SCADJ	PAM8301AAF	PAM8945PJR
AL8843SP-13	AP2210N-3.3TRG1	PAM2421AECADJR	PAM8302AADCR	SMAJ5.0A-13-F
AL8860MP-13	AP3012KTR-G1	PAM2423AECADJR	PAM8302AASCR	ZXMP10A13FTA
AL8860WT-7	AP4310AMTR-G1	PAM2803AAF095	PAM8303DBSC	PT7C4302WEX
AL8861WT-7	AP4313KTR-G1	PAM2804AAB010	PAM8304ASR	PT7C4337UEX
AL8861Y-13	AP7333-33SAG-7	PAM2808BLBR	PAM8320RDR	PT7C4337WEX

深圳市致新科科技有限公司

Shenzhen Zhixinke Technology Co., Ltd.



微盟 (Microne)

ME1117 MET1117	ME3116AM6G	ME431BXG	ME6210	ME8115BD7G	
ME1502CM5G	ME321AM5G	ME6118A33B3G	ME6211	ME8115D7G	
ME2107A50M5G	ME358ASG	ME6119C33M5G	ME6212	ME8125AS6G	
ME2108	ME4054BM5G	ME6203A50M3G	ME6213C33M5G	ME8165GD8G	
ME2188	ME4055AM6G	ME6206	ME6214C18M5G	ME8202SG	
ME2214AM6G	ME4056SPG	ME6206A33M3G	ME6215C25M5G	ME8321AS7G	
ME2807A30M3G	ME4074AM5G	ME6208	ME6216A30XG	ME8327BS7G-N	
ME3102BM5G	ME4211AM6G	ME6209	ME6228	MEL7135PG-N	
ME3110AM6G	ME4313CM6G	ME6209A50M3G	ME6230	MEL7136AP5G	
恩智浦(NXP) 安世	半导体(NXPERIA)				

2N7002	74HC238PW	74HC574D	BCX51-16	HEF4094BT	
74HC00D	74HC245D	74HC595D	BT137-800E	HEF4511BT	
74HC04D	74HC245DB	74HC595N	BT139-800E	PCF8563T	
74HC08D	74HC245N	74HC74D	BT151-500R	PCF8563T/5	
74HC125D	74HC245PW	74HC86D	HEF4001BP	PCF8563TS/5	
74HC138D	74HC257D	74HCT164D	HEF40106BP	PMBT3904	
74HC138PW	74HC373N	74HCU04D	HEF4011BP	PMBT3906	
74HC14D	74HC393D	BA591	HEF4011BT	PRTR5V0U2X	
74HC154D	74HC4051D	BAT54	HEF4012BP	TJA1021T	
74HC157D	74HC4051PW	BAV199	HEF4013BP	TJA1027T	
74HC164D	74HC4066D	BAV99	HEF4013BT	TJA1040T	
74HC164PW	74HC4316D	BC817-40	HEF4051BT	TJA1042T	
74HC165D	74HC4538D	BC846B	HEF4069UBT	TJA1044T	
74HC238D	74HC573D	BC858B	HEF4093BP	TJA1050T	
6+ 111 (), HH (m=a)					

德州仪器(TIS)

CD14538BE	LM2576S	NE5532	SN74HC273	TLV75718PDBVR
CD4001BE	LM258DGKR	OPO7CDR	SN74HC595	TLV75728PDBVR
CD40106BE	LM2596SX	OPO7CP	SN74LVC1G08DCKR	TPA3116D2
CD4011BE	LM2901	PCA9306DCUR	SN74LVC1G175DCKR	TPS23881RTQR
CD4012BE	LM2902	SN65C1168ERGYR	SN74LVC1G3157DBVR	TPS2412PWR
CD4013BE	LM2903	SN65HVD230DR	SN74LVC1G32DRLR	TPS54331DDAR
CD4017BM96	LM2904	SN65HVD231DR	SN74LVC2G07DBVR	TPS54620RGYR
CD4026BE	LM317	SN65LBC184	SN74LVC2T45DCUR	TPS62291DRVR
CD4050	LM321	SN74AHC1G08DBVR	TL081CP	TPS62410DRCR
CD4051	LM324	SN74AHC1G86DCK	TL082BCDR	TPS63000DRCR
CD4052	LM339	SN74AHC1GU04DRLR	TL084CN	TPS63020DSJR
CD4053	LM358	SN74AVC16T245DGGR	TL431	TPS76330DBVR
CD4069UBE	LM393	SN74HC04	TL494CDR	TSS721ADR
CD4081BE	LMV321IDBVR	SN74HC138	TLC272CDR	TXS0102DCUR
CD74HC221M96	LMV324ID	SN74HC14	TLC274CD	UCC28070PWR
DRV8837DSGR	MAX202	SN74HC148	TLV272CDR	UCC28180
L298N	MAX232	SN74HC165	TLV62569DBVR	ULN2003
LM224DR	MAX3232	SN74HC244	TLV70033DDCR	ULN2004
会外水 自体 (cmr)				

意法半导体(STM)

₩ (DIM)				
BTA08-600CRG	L78L05ACUTR	M24C64-RMN6TP	STM32F207ZET6	STM8S103F3P6
BTA08-800CRG	L78MO5CDT	ST1S10PHR	STM32F401CEU6	STM8S103K3T6C
BTB04-600SL	L78M08ABDT	STM32F030C6T6	STM32F405RGT6	STM8S105C6T6
HCF4052M013TR	LM258AD	STM32F030C8T6	STM32F407VET6	STM8S105K4T6C
L298N	LM2903	STM32F030F4P6	STM32F407VGT6	STM8S105S4T6C
L6562DTR	LM2904	STM32F030K6T6	STM32F407ZET6	STM8S105S6T6
L6599ATDTR	LM293	STM32F051C8T6	STM32F407ZGT6	STM8S207RBT6
L7805CDT	LM317T	STM32F071VBT6	STM32F429IET6	TDA2030AV
L7805CV	LM324	STM32F103C8T6	STM32G070RBT6	TDA7265
L7806CV	LM335	STM32F103R8T6	STM32L475VET6	TDA7851L
L7809CV	LM339	STM32F103RCT6	STM8L051F3P6	TIP122
L7812CV	LM358	STM32F103VCT6	STM8L052C6T6	VIPER12ADIP-E
L7815CD2T-TR	LM393	STM32F105RBT6	STM8S003F3P6	VIPER17LN
L78L05ABUTR	M24C02-WMN6TP	STM32F107VCT6	STM8S005K6T6C	VIPER22ASTR

深圳市致新科科技有限公司 Shenzhen Zhixinke Technology Co., Ltd.



安森美(ONS) 仙童(FAIRCHILD)

安森美(ONS) 仙堇(I	FAIRCHILD)			
6N137	LM339DR2G	MC33063ADR2G	MC78M08CDTRKG	MMBT3906LT1G
LM2902DR2G	LM393DR2G	MC34063ADR2G	MC7915CD2TR4G	MMBT8550LT1G
LM2903DR2G	LM358DR2G	MC7805	MC7915CTG	SG3525ANG
LM2904DR2G	MBR20100CTG	MC7812CDTRKG	MC79MO5BDTRKG	UC2843BNG
LM317LBDR2G	MBRS340T3G	MC7815CTG	MC79M15CDTRKG	UC2844BD1R2G
LM324DR2G	MBRS540T3G	MC78L05ACDR2G	MMBT3904LT1G	UC3845BNG
MAXLINEAR 艾科嘉(EXAR) 西伯斯(SIPEX)	'		
SP202EEN-L/TR	SP3222EEA-L/TR	SP3243EUEA-L/TR	SP485EEN-L/TR	SPX5205M5-L-3.3/TR
SP232EEN-L/TR	SP3232EBEA-L/TR	SP336EEY-L/TR	SPX29302T5-L/TR	SPX5205M5-L-5.0/TR
SP3220EEY-L/TR	SP3232EEY-L/TR	SP3485EN-L/TR	SPX3819M5-L-3-3/TR	SPX1117
新日本无线(JRC)		<u> </u>		
NJM2035M	NJM2370U33	NJM2831F33	NJM3414AM	NJM78M05DL1A
NJM2274R	NJM2567V	NJM3404AV	NJM4558M	NJM79M05DL1A
美信(MAXIM) 达拉期				
DS1302	DS1337	MAX232AEPE	MAX232CSE	MAX3232IPWR
DS1307	MAX17126ETM	MAX232AEPE	MAX232ESE	MAX485ESA
DS1338Z	MAX1771CSA	MAX232AESE	MAX232N	MAX6701BAUT30
DS2431P	MAX202CPW	MAX232CPE	MAX3088ESA	MAX9722AETE
微芯(MICROCHIP) 爱				
AT24C02C-SSHM-T	AT24C64D-SSHM-T	PIC16F1936-I/S0	PIC16F505-I/SL	PIC16F723A-I/SS
AT24C04C-SSHM-T	PIC12F1822-I/SN	PIC16F1938-I/S0	PIC16F54-I/S0	PIC16F723-I/S0
AT24C16C-SSHM-T	PIC12F508-I/P	PIC16F1938-I/SS	PIC16F676-I/SL	PIC16F883-I/SS
AT24C256C-SSHL-T	PIC16F1826-I/S0	PIC16F1947-I/PT	PIC16F722A-I/SS	PIC16F914-I/PT
STC	1101011020 1, 50	1 101011011 1/11	1101011-11111111	1 10101011 1,11
STC15W4K32S4	STC12C5A32S2	STC15W204S	STC8A8K48D4	STC8H1K08
STC13#4K3234 STC8H3K64S4	STC12C5A32S2	STC15W404AS	STC8A8K64D4	STC8H3K32S2
STC11L32XE	STC12C5A56S2	STC15W4K32S4	STC8A8K64S4A12	STC8H3K48S
STC11L60XE	STC15F2K08S2	STC15W4K48S4	STC8F1K08S2	STC8H3K48S4
STC12C5604AD	STC15L204EA	STC89C55RD	STC8F2K16S2	STC8H8K48U
STC12C5A08AD	STC15W104	STC8A8K32S4A12	STC8G1K08A	STC8H8K64U
华邦(WINBOND)	510101101	STOOMOROUS INTE	orcoomoon	5 Tooliono To
W25Q128FVSIG	W25Q128JVSIQ	W25Q128JWPIQ	W25Q16JVSSIQ	W25Q32JWSNIQ
	#29&120J\21&	WZJ&1Z0JWI1W	#20Q10J1331Q	#ZJQJZJ#JNIQ
美国芯源(MPS)	WD 4 0 = 0 0 m D	WD00004DW 4 D G	MD COORD B	VD0==000 G
MP1471AGJ-Z	MP1653GTF-Z	MP2303ADN-LF-Z	MP2636GR-Z	MP8756GD-Z
MP1482DS-LF-Z	MP1657GTF-Z	MP2359DJ-LF-Z	MP3202DJ-LF-Z	MP9447GL-Z
MP1484EN-LF-Z	MP1658GTF-Z	MP2374DS-LF-Z	MP3426DL-LF-Z	MP9495DJ-LF-Z
MP1494DJ-LF-Z	MP2015AGG-33-Z	MP24943DN-LF-Z	MP5013AGJ-Z	MP9518GJS
MP1601GTF-Z	MP2122GJ-Z	MP26029GTF	MP6650GJS	NB679GD-Z
MP1605GTF-Z	MP2144GJ-Z	MP2603EJ-LF-Z	MP8126DF-LF-Z	NB680GD-Z
昂宝电子(On-Bright		ana a a un	- Innecessing	00000000
OB3635	OB2222MCP	OB2263MP	OB2281MP	OB2535CPA
OB2212AP	OB2263AP	OB2273AMP	OB2356LCPA	OB3636MP
电池芯片 马达驱动				
4054 SOT23-5	CW1053	HP4011	LN8238A	TC118
4056 ESOP8	DWO2R	HY2213	FM8002A	TC618CS
CW1051	DW06D	IP5305	TC117HS	TMI8118S
其它IC				
RTL8201CP-VD-LF	IT7C4337WEX	IT8563UEX	HYM8563	TH10CA061
RTL8201F-VB-CG	IT8563WEX	BM8563	AiP8563	TH11CA031

我司本着"质量为第一"的理念,通过正规渠道采购物料,专业采购师对采购物料要求严格,

保证质量,在业界获得好评,货源优秀,港深两地常备原装现货。买原装正品IC,找致新科。